Abstract

A time division multiplex data recovery system using a closed-loop phase lock loop(PLL) and delay locked loop(DLL) is disclosed. In other words, one closed loop comprises both a phase locked loop (PLL) and a delay locked loop (DLL) in a novel time division multiplex data recovery system. This new architecture comprises a 4 stage Voltage Controlled Oscillator (VCO) used to generate 8 clock signals, 45 degrees phase shifted from one another, for 8 receivers 41 to do the oversampling. An interpolator tracks the received data signal and feeds it back to the Phase/Frequency Detector (PFD). The PFD has a second input of the reference clock which the PFD uses along with the interpolator input to correct the frequency of the PLL. The PLL operates at a high bandwidth. The DLL's bandwidth is several orders lower than the PLL. The DLL activates only a multiplexer and an interpolator continuously, thereby drawing a minimum amount of power.